AN2870
Application note

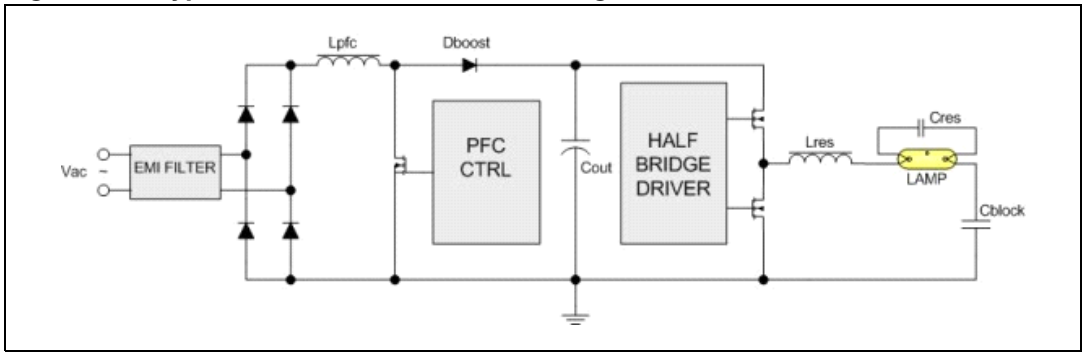
L6585DE combo IC

Introduction

The modern requirements for fluorescent lamp electronics ballast concerns both efficiency of the drivers and safety aspects.

The L6585DE offers the designer a high performance PFC stage, high capability half bridge high voltage drivers, a fully programmable control and an enhanced set of protections.

Figure 1. Typical electronic ballast block diagram



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1 Introduction

1.1 Typical configuration

Typical fluorescent lamp electronic ballasts are composed by (*Figure 1*):

- An input PFC section, if input power is greater than 25 W, usually a TM PFC converter, that generates a DC output voltage and absorbs power from mains with very high Power Factor (typically 0.95 or grater) and very low THD (mandatory less than 10%).
- A high frequency half bridge driver, fed by the PFC output, with internal or external oscillator, a timer and various protections in order to drive correctly the lamp, to avoid to deliver an excessive power to the lamp and to detect any malfunction of the lamp (broken lamp, broken cathode or lamp absence)
- An output resonant stage, realized by reactive components (capacitors and inductors), that, together with the half bridge driver, optimizes the power delivered to the lamp (one or more) during all working conditions (preheating, ignition and run mode).

1.2 Lamp requirements

Fluorescent lamp, during its normal operation, has to be supplied by means of alternative and controlled current. In order to reduce the size of the ballast and increase the light efficiency of the lamp a frequency greater than 20 kHz is typically used. A half bridge quasi resonant inverter (series-parallel converter *Figure 1*) is used to obtain sinusoidal current into the lamp and to reduce the power dissipation of the half bridge switches, in fact zero voltage switching is achieved.

Lamp current and lamp voltage during normal operation are reported in lamp documentation and are to be considered as design specification. Moreover, a well preheated lamp ignites at a lower voltage; this implies a longer lamp life and a greater number of ignitions. The efficiency of the preheating is mainly related with the total energy delivered to the cathode (reported on lamp documentation), and then it depends on the time available for this operation: keeping constant the preheating energy, longer is the preheating time, smaller is the instantaneous power delivered to the cathode. During the preheating operation the voltage across the lamp must be kept below a specified value in order to avoid unwanted ignitions (when these happen, the lamp experiences multiple re-strike and dissipates large amounts of power).

There are many ways to deliver power to the cathode, but the most used are two:

1. Current controlled preheating: the cathodes are interposed between the choke and the resonant capacitor so they experience the same current of the resonant LC circuitry. An efficient preheating is obtained controlling this current and the time of preheating. The advantages of this method are the cheapness and easiness of design; it has also some disadvantages, namely the difficulty of keeping low the lamp voltage during preheating and the fact that during steady state the cathode experiences the sum of the lamp current and of the resonant capacitor current.
2. Voltage controlled preheating: the current into the cathodes is generated by auxiliary windings coupled with ballast choke or driven by an auxiliary oscillator. This implies that, in any case, the design of the preheating circuitry is somewhat independent from the design of the LC circuitry, even if it requires a lot of external components. This method is then more efficient, but is cheaper and more difficult to design.

After a good preheating, the voltage across the lamp is suddenly increased in order to generate a strike inside the tube and ignite the lamp. This phase should last between 10 ms and 100 ms.

The strike voltage depends on various parameters, many of which cannot be exactly evaluated: preheating energy, remaining lamp life, number and efficiency of the past ignitions. An insufficient preheating causes greater ignition voltage and a subsequent stress of the cathodes that lose small amounts of material that darken the region of the tube near to the cathode itself (sputtering).

Lamp ageing is related with the symmetrical or, more often, asymmetrical increasing of the cathodes resistance. A symmetrically aged lamp absorbs more power causing hard switching and over-current. Asymmetrically aged lamps experience a current that is more intense in one direction than in the other. This implies that the current flowing into the lamp has positive or negative mean value (DC component). This effect can be detected measuring the mean values of the lamp voltage that should be zero in normal lamps. The worst case of rectifying effect causes the current flowing only in one direction: the voltage across the resonant capacitor can reach very high values and heavy hard switching is detected.

When symmetrical or asymmetrical ageing of the lamp reaches a value indicated in international norms, the lamp reaches its end of life (EOL).

2 L6585DE combo IC

The L6585DE embeds both a PFC converter and a ballast regulator in a single SO20 package. It is intended to design complete high power electronic ballasts with a single chip.

- The most significant features of the L6585DE concern the following points:
- Transition mode PFC converter with over voltage and over current protection.
- Half-bridge controller with High voltage driver (600 Vdc) and integrated bootstrap diode.
- 3% precise, fully programmable oscillator.
- Flexibility in programming preheating time and ignition time.
- Configurable EOL detection and over current protection.
- Hard switching detection.

The PFC section achieves current mode control operating in Transition Mode. The multiplier, together with the internal THD optimizer, reduces input current distortion, and allows reaching very high performances also in wide-range-mains operation and large load range. The PFC output voltage is controlled by means of a voltage-mode error amplifier and a precise internal voltage reference.

A static and dynamic OVP protects the IC from excessive output voltage and an over current protection turns off the PFC gate driver in case of PFC choke saturation.

The PFC driver is able to provide 300 mA (source) and 600 mA (sink).

The half bridge section is driven by a current controlled oscillator (CCO) and the internal control logic.

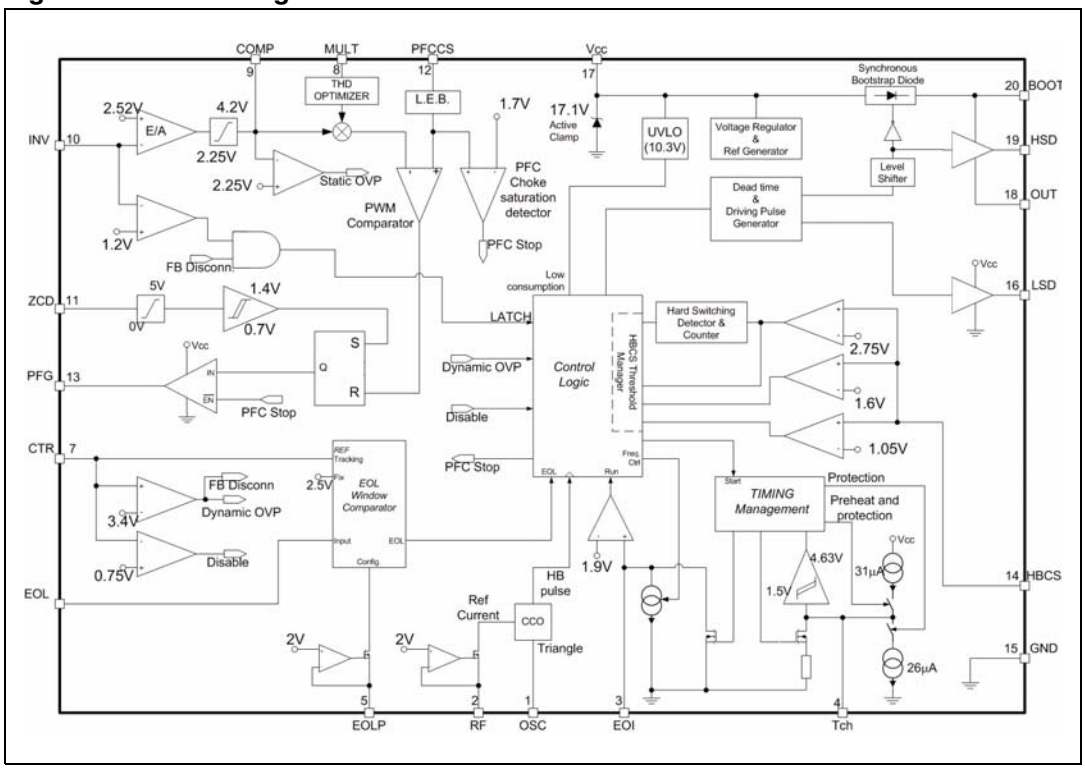
The steady state frequency, the preheating frequency, the pre-heating time, the over-current protection time and the ignition time are independently set by means of six external components (resistors and capacitors).

An over-current protection limits the voltage across the HBCS pin acting directly on the CCO realizing a precise closed loop control. This control lasts for a time set by the Tch pin and, after that, if the fault condition is still present, the IC is stopped in low consumption mode. The HBCS voltage amplitude depends on actual operating mode, then this protection can detect either a broken lamp during ignition (in this case the current regulation implies the lamp voltage regulation) or the symmetrical ageing of the lamp during run mode.

An internal window comparator can be simply configured setting the window amplitude or the comparator reference in order to detect the EOL status. The programmability of comparator reference makes the L6585DE compliant with either “lamp-to-ground” (fixed reference) or “block capacitor-to ground” (tracking with CTR) configurations.

The drivers of the half-bridge provide 290 mA source and 480 mA sink.

Figure 2. Block diagram



3 Device blocks description

3.1 Start-up and shut-down

During start-up the chip is supplied through a resistive path from the rectified AC Mains voltage whereas, during normal operation, a self-supply source is recommended: a charge pump, an auxiliary winding coupled either with PFC choke or resonant choke, or an auxiliary converter.

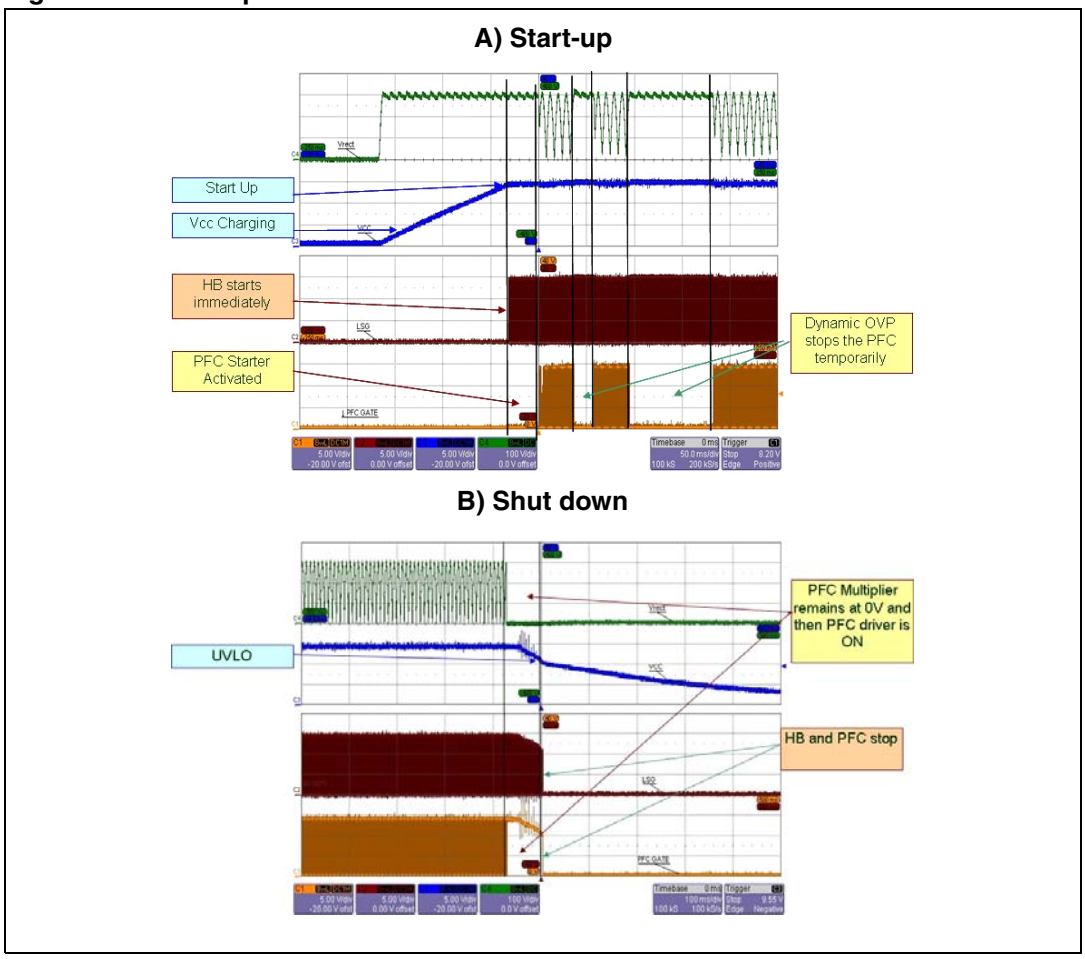
As the voltage at Vcc pin reaches the turn-on threshold (Vcc_{ON}, *Figure 3*-A), the chip is enabled and (unless a lamp absence is detected) the Half-Bridge and the PFC sections start at the same time (independently):

- The PFC section, as the synchronization signal at pin ZCD is not yet generated by the external ZCD circuit, is forced to switch by internal starter ($f_{starter}$ = 6 kHz (typ)) for the first few switching cycles, until the control loop operates correctly at a frequency higher than $f_{starter}$.
- The oscillator starts switching at a preheating frequency set by values of C_{OSC}, R_{RUN} and R_{PRE}.

At shut-down (*Figure 3*-B), when the V_{CC} decreases below the UVLO threshold (either in case of mains removal or in case of fault):

- All drivers are off;
- EOI pin is discharged (the internal switch is on);
- RF reference is disabled;
- Tch is discharged.

Figure 3. Start-up and shut-down waveforms



3.2 PFC section

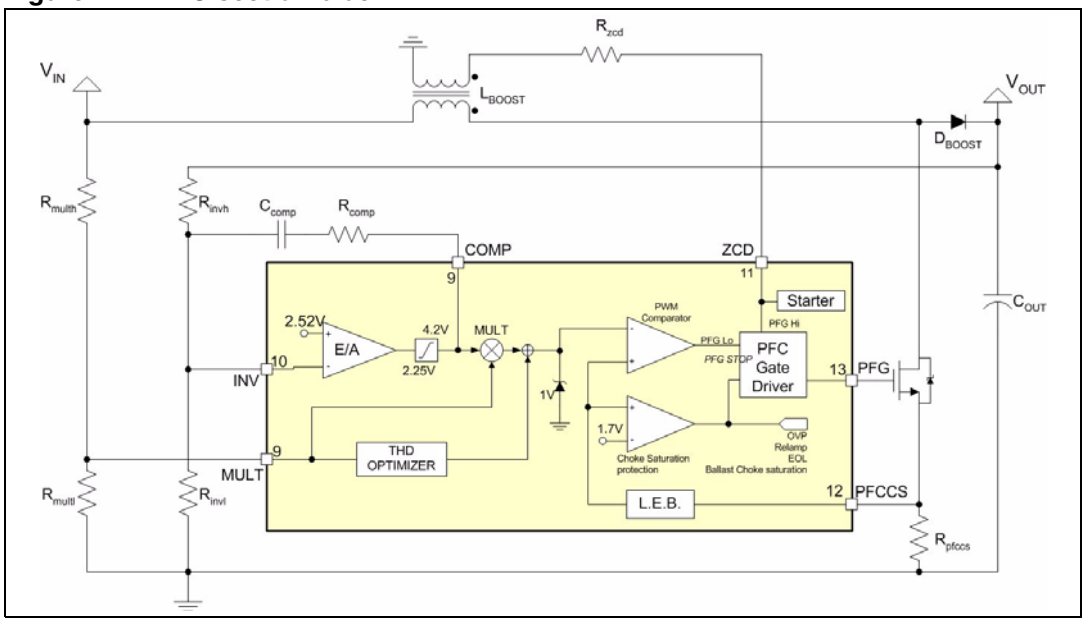
3.2.1 Error amplifier

The error amplifier (E/A, *Figure 4*) is used to close the output voltage control loop. Its non inverting input is connected to a precise voltage reference (2.52 V), the inverting input and the output are externally available (pin 10 –INV; pin 9 – COMP).

The compensation network, placed between pins INV and COMP, is needed to reject the mains ripple.

The E/A output dynamic is internally clamped: it can swing between 2.25 V and 4.2 V in order to speed up the recovery after the E/A saturates low due to an over-voltage (static OVP) or saturates high because of an over-current.

Figure 4. PFC section block



3.2.2 Multiplier block and THD optimizer

The multiplier (*Figure 4*) gives the sinusoidal voltage reference to the current sense in order to absorb from the mains a sinusoidal current. This current will be function of both input voltage and load current then this block has two inputs: the first one (Pin MULT – 8) takes a partition of the instantaneous rectified line voltage and the second one (Pin COMP – 9) is the output of the E/A.

An internal voltage clamp (1 V) sets the maximum allowed voltage of the multiplier output, then it act as PFC current limiter.

When the rectified input voltage reaches 0 V the boost inductor cannot store enough energy to discharge the input capacitor: this event increases the THD. In order to avoid this additional distortion, a THD optimizer block is placed between the output of the multiplier and the current sense comparator.

The characteristic curves of the multiplier block are reported in *Figure 14*.

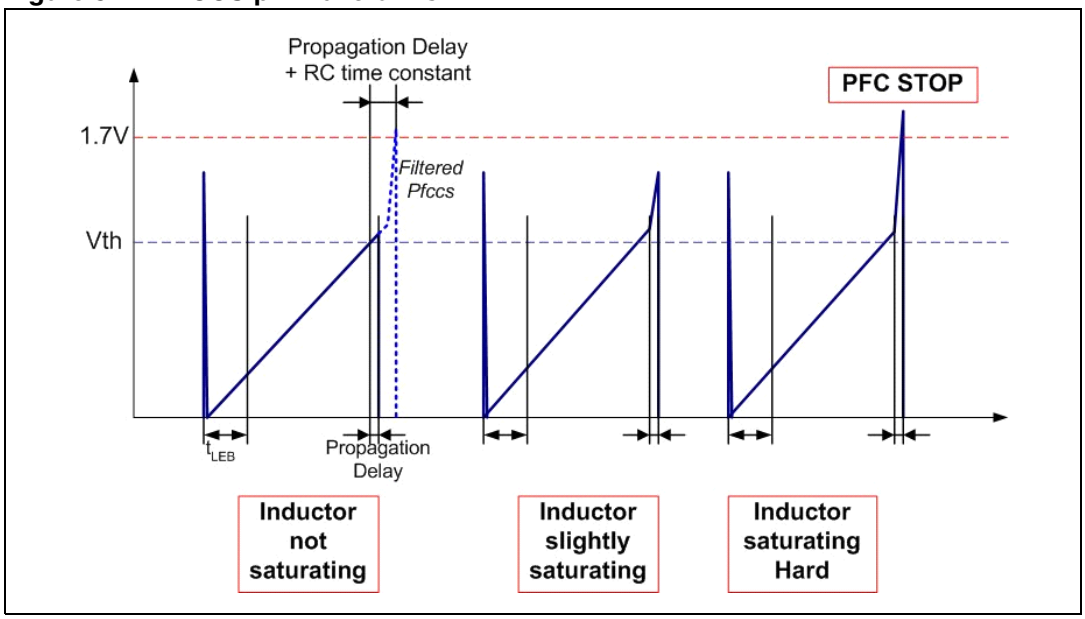
3.2.3 Current comparator and choke saturation detection

The current comparator senses the voltage across the current sense resistor (R_{pfccs}) and, by comparing it with the programming signal delivered by the multiplier, determines the exact time when the external MOSFET has to be switched off.

When PFC MOSFET is turned on, parasitic drain capacitances are discharged and an intense current spike can be seen by PFCCS (*Figure 5*). In past solutions, an RC filter between sense resistor and current sense input was commonly used to reject these spikes, but it introduced a delay between the instant the current crosses the threshold and the actual activation of internal comparator. This delay may cause the inductor saturation, then an over dimensioned inductor had to be used. In L6585DE, an internal leading edge blanking structure (LEB) masks the first 200 ns of the PFC gate at the time current spikes occurs; the filter is no longer necessary and the inductor can be smaller and lighter. On the other hand this LEB limits the maximum available “ON time”.

Moreover, the device is provided with a second comparator on the PFC current sense pin that turns off immediately the PFC MOSFET if the voltage on the pin, normally limited within 1.0 V, exceeds 1.7 V. A current peak limiting control is therefore achieved avoiding MOSFET overheating in case of boost inductor’s hard saturation. In this case the current up-slope becomes so large (50-100 times steeper) that during the current sense propagation delay the current may reach abnormally high values.

Figure 5. PFCCS pin waveforms



3.2.4 Zero current detection

The zero current detection (ZCD) block switches on the external PFC MOSFET as the current through the boost inductor has gone to zero. This feature allows TM operation.

When the circuit is running, the signal for ZCD is obtained with an auxiliary winding coupled with the boost inductor. A Schmidt trigger prevents false activations and an internal clamp limits the voltage across the pin during normal operation in 0 V-5 V range. As at start-up no signal is coming from the ZCD, an internal starter is needed in order to turn on the external MOSFET and to arm the ZCD trigger.

The repetition rate of the starter is ≅ 6 kHz and this maximum frequency must be taken into account at design time.

3.2.5 Driver

A totem pole buffer, with 300 mA source and 600 mA sink capability, allows driving an external MOSFET. A pull-down circuit holds the output low when the device is in UVLO conditions, to ensure that the external MOSFET cannot be turned on accidentally.

3.2.6 PFC protections

The device is provided with a double over-voltage protection (OVP).

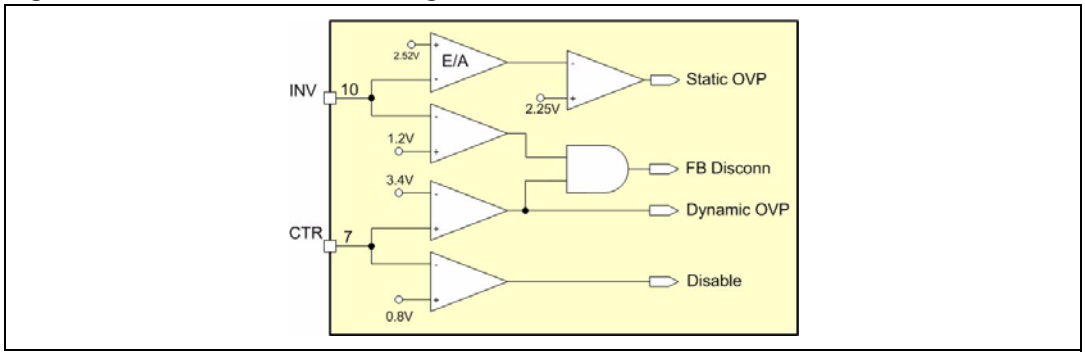
The first over voltage protection, also called dynamic OVP, is activated immediately when CTR pin (pin 7) goes above 3.4 V. The maximum voltage allowed for the output voltage (V_{OVP}) is defined by a resistive divider connected between output voltage and CTR pin.

In case of over voltage, the output of the E/A will tend to saturate low with a long constant time, because of the bandwidth of this stage (typ. 10 Hz).

If the over-voltage lasts so long that the output of E/A goes below 2.25 V, the PF gate driver is stopped and Tch timer is started. If E/A output voltage doesn't return above 2.25 V after the timer finishes its count, the IC is stopped in latch condition. This protection prevents damages due to the connection to an excessive input voltage.

An intense high voltage (e.g. a surge) may break the upper resistors (one or more than one) of the voltage dividers connected to input voltage (MULT biasing) or to output voltage (INV and CTR biasing). Losing of the bias on pin INV implies losing of the control of the loop: in fact E/A output saturates high and causes an increased output voltage, eventually not seen by OVP because of failure on CTR voltage divider. The feedback disconnection protection prevents this failure stopping the PF gate if INV voltage falls below 1.2 V and CTR pin goes above 3.4 V. CTR pin can be also used to disable the IC pulling its voltage below 0.8 V.

Figure 6. Protections block diagram



3.3 Ballast controller section

3.3.1 Oscillator and timer

The half bridge driver oscillation is regulated by a current controlled oscillator (CCO): it needs a capacitor connected to OSC pin (pin 1) and uses the current flowing outside RF pin (pin 2) as reference.

The RF pin has a 2 V precise voltage reference that let the designer fix the run mode frequency simply connecting a resistor between RF pin and GND (Rrun).

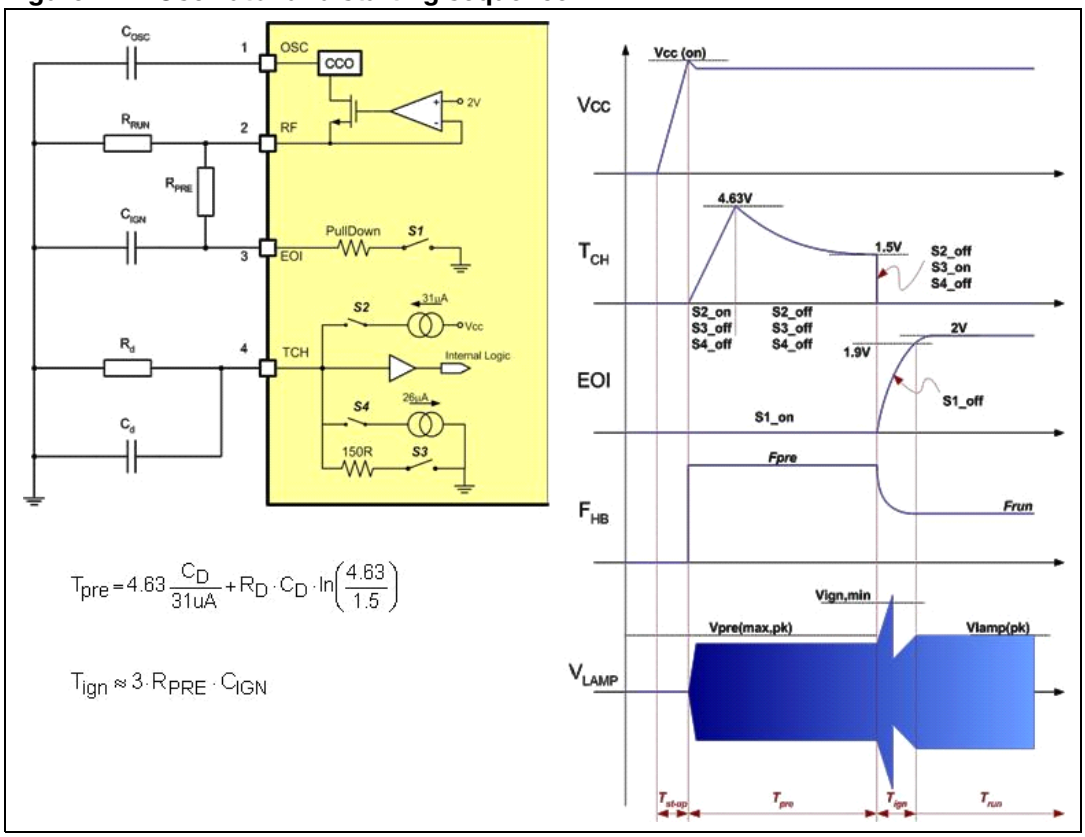
The EOI pin (pin 3) is driven by the internal logic in order to set the frequency during the preheating and to control the lamp current during an over-current event in the half bridge.

Preheating frequency is set by the parallel of Rrun and a resistor (Rpre) placed between RF and EOI: in fact during the preheating the EOI pin is pulled to GND.

TCH pin is connected to the parallel of a resistor (R_D) and a capacitor (C_D) and is used in order to define the preheating time and the protection time; its cycle (Tch cycle) is composed by the following steps:

1. A 31 µA current generator charges the C_D causing TCH voltage to rise linearly,
2. When TCH voltage reaches 4.63 V, the TCH pin is left in high impedance status and C_D is discharged by R_D,
3. When TCH voltage reaches 1.5 V the cycle finishes and an internal resistor pulls down the TCH pin to GND.

Figure 7. Oscillator and starting sequence



$$T_{pre} = 4.63 \frac{C_D}{31uA} + R_D \cdot C_D \cdot \ln\left(\frac{4.63}{1.5}\right)$$

$$T_{ign} \approx 3 \cdot R_{PRE} \cdot C_{IGN}$$

3.3.2 Overcurrent control and protections

Limiting the current flowing into the half bridge:

- The lamp voltage during the ignition phase is limited
- The power of the lamp during run mode is limited

Ignition phase: (see *Figure 8*) if the VHBCS high threshold (HBCSH = 1.6 V) is crossed (because the lamp doesn't ignite), the following actions are taken by L6585DE:

1. A current, whose amplitude is proportional to the time the V_{HBCS} is above threshold, is sunk from EOI and consequently from RF pin. This results in a frequency increase that reduces the resonant network current and therefore the lamp voltage.
2. A reduced time is calculated by Tch pin:
   a) The 31µA generator charges C_D to 4.63 V
   b) Instead of leaving C_D to be discharged by R_D, a 26 µA current generator discharge quickly C_D to 1.5 V (S4 on)
   c) The pull down switch S3 completes the reduced cycle

The reduced Tch cycle depends only on C_D value and is equal to:

Equation 1

$$T_{Tch,reduced} = C_D\left(\frac{4.63}{I_{Tch,source}} + \frac{4.63-1.5}{I_{Tch,snk}}\right) \cong 269740 \cdot C_D$$

At the end of the Tch cycle, during the first subsequent low side on time, the HBCS voltage is checked: if V_{HBCS} is higher than a threshold ($HBCS_{H,test}$) the IC is stopped in latched condition, otherwise EOI pin is released in high impedance status. When EOI voltage reaches 1.9 V the IC enters the run mode.

The sense resistor value defines the maximum current that can flow during ignition and then the maximum allowed lamp voltage.

The linear growth of the lamp voltage, thanks to the exponential decrease of the operating frequency during ignition allows a better control of the voltage thanks to a lower dV/dF_{sw}.

In case of choke saturation the intense current results in very high V_{HBCS}. The 2.75 threshold triggers this event and stops immediately the IC.

Run mode: During this phase, current control similar to the one present during ignition is available in case of an over-current due to symmetrical ageing of the lamp. It follows the same rules, but the threshold is equal to 1.05 V instead of 1.6 V.

Also during *run mode* the saturation protection is active: in case of choke saturation due to lamp breaking, lamp removal and capacitive mode where V_{HBCS} experiences a spike whose amplitude is higher than 1.6 V and whose duration is longer than 300 ns. This kind of event causes the IC turn-off in latched condition.

The lamp ageing causes the shift of peak of the resonance curve towards the run frequency. This results in hard switching behavior: the half bridge doesn't work at ZVS and spikes appears at HBCS pin. These spikes have very high amplitude (up to 8 V) and short duration (30 ns-50 ns).

During hard switching the power dissipation of half bridge MOSFETs increases rapidly. L6585DE detects these pulses and shuts down the half bridge after 350 (typ) subsequent pulses.

The hard switching detection structure is masked during preheating and ignition: in fact during this phase the frequency changes cause hard switching that is unavoidable but is not dangerous.

In *Figure 9* a summary of the protection thresholds is reported:

Figure 8. Current control sequence during ignition

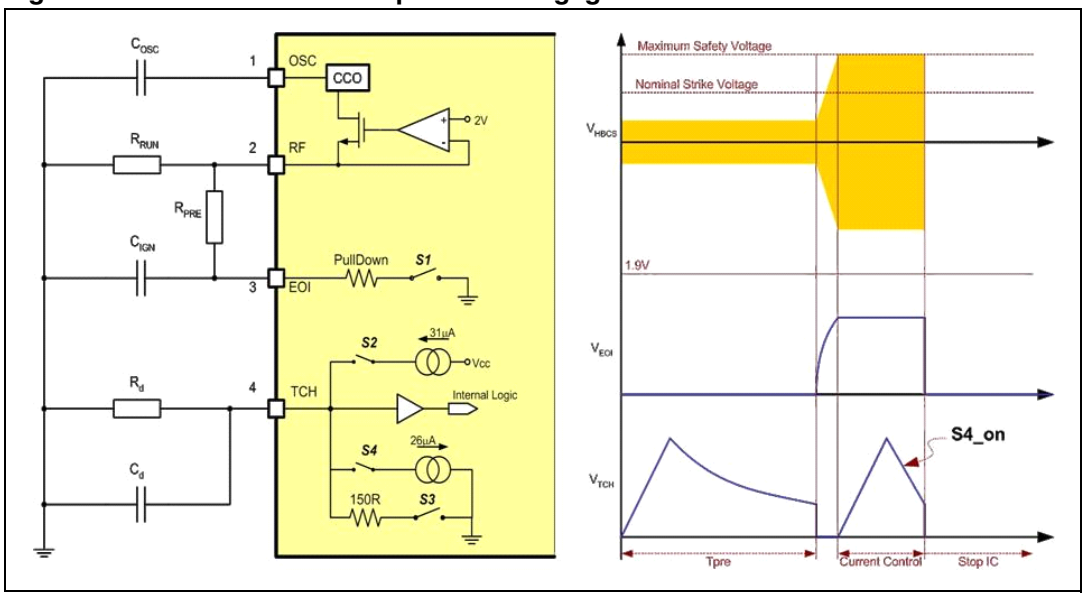
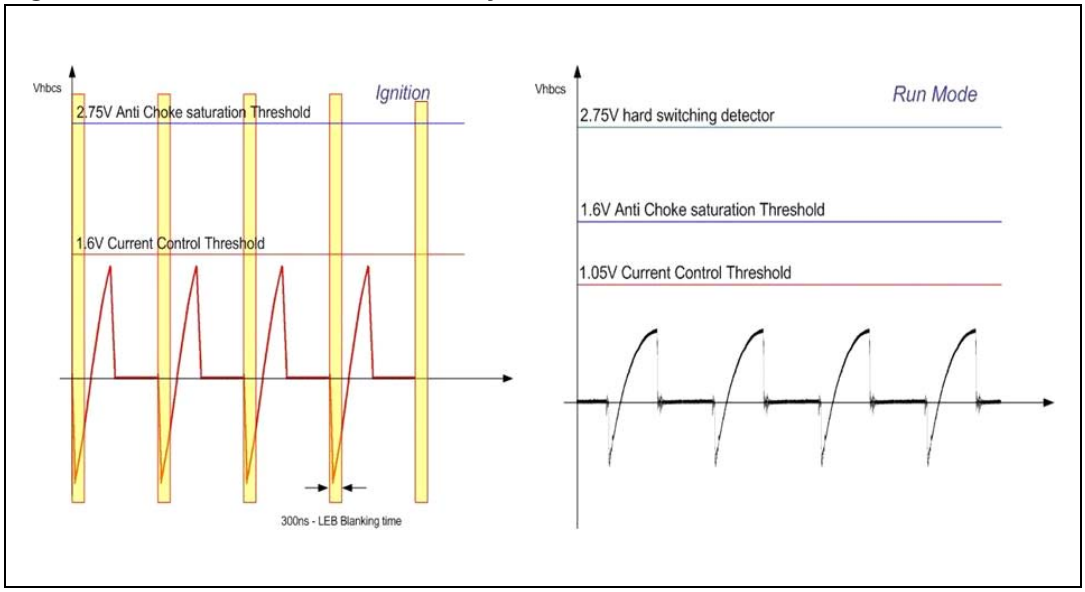


Figure 9. HBCS thresholds summary



3.3.3 End of life detection

When the lamp becomes older and approaches its end of life, its equivalent resistance increases symmetrically or asymmetrically.

In symmetrical ageing a modification of the frequency response of the resonance network can be seen and, consequently, an increasing of lamp current and the appearance of hard switching events: in fact the resonance frequency is now closer to operating frequency.

In asymmetrical ageing the current flowing in one direction is greater than the current flowing in the other; this means that lamp voltage and current waveforms have no longer zero mean value. A window comparator measures the variation of the DC component of the lamp voltage that can be either positive or negative. The reference and the amplitude of this comparator can be set choosing the value of a resistor connected between EOLP pin and GND accordingly with the following table.

Table 1. Comparator amplitude

EOLP resistor	Symbol	Reference	Half–window amplitude
R_{EOLP} > 620 kΩ	R_{FH}	Fixed 2.5 V	± 720 mV
220 kΩ < R_{EOLP} < 270 kΩ	R_{TL}	Tracking with CTR	- 240 mV / + 250 mV
75 kΩ < R_{EOLP} < 91 kΩ	R_{FL}	Fixed 2.5 V	± 240 mV
22 kΩ < R_{EOLP} < 27 kΩ	R_{TL}	Tracking with CTR	- 150 mV / + 160 mV

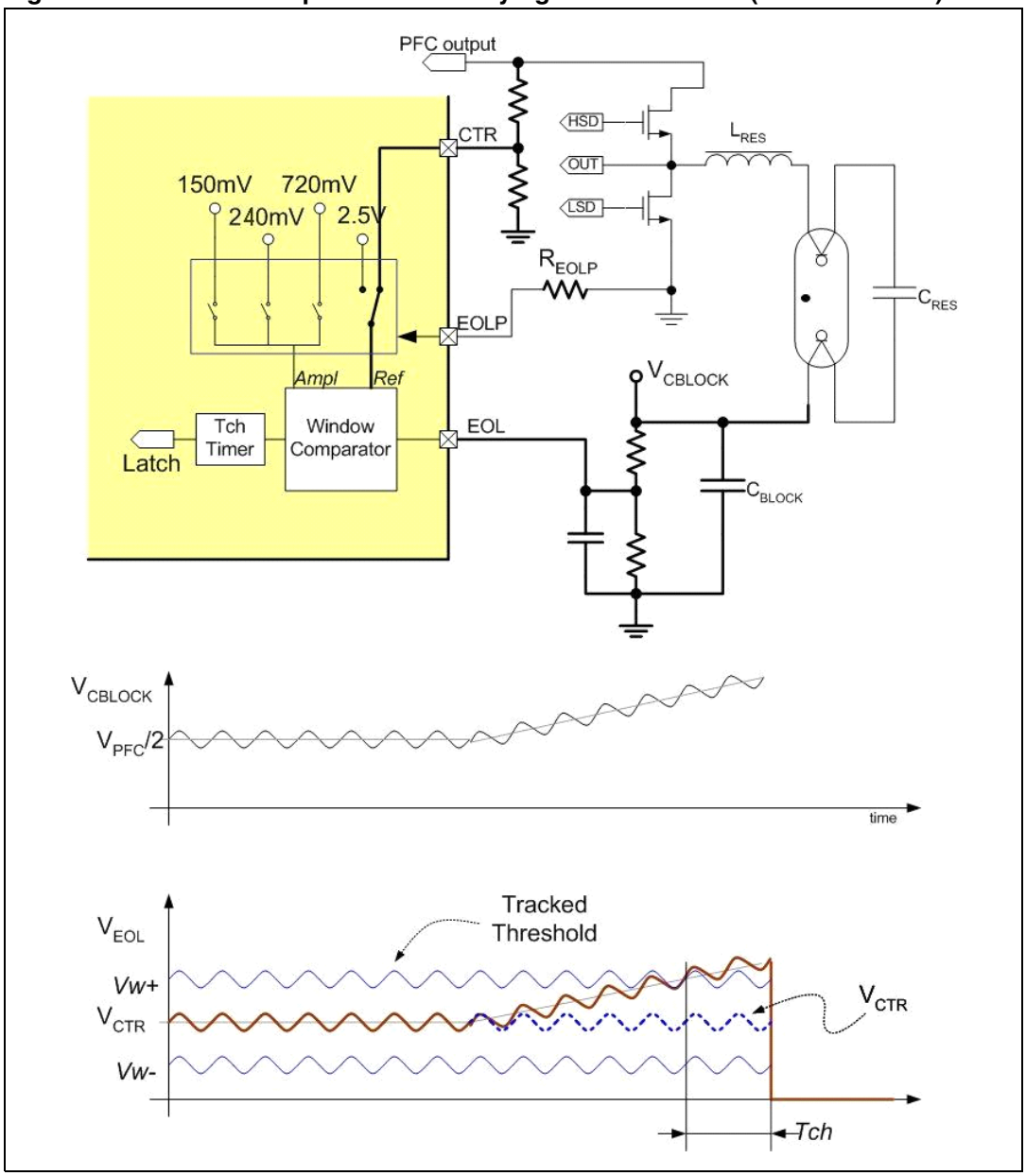
This comparator can be used in both the two most used ballast configurations: Blocking capacitor to ground and lamp to ground.

Block capacitor to ground (*Figure 10*): During normal operation the DC mean value across Cblock is equal to the half of the output voltage of the PFC. A resistive divider is placed across the block capacitor to sense its DC voltage: the asymmetric effect appears as a shifting of this DC value.

Any voltage ripple or disturbance across the output voltage is present also on Blocking Capacitor and may alter the correct detection of a lamp at the end of its life.

In order to reject all this disturbances, the reference of the window comparator is connected to CTR pin (Tracking reference configurations): in fact this pin is connected directly to the output voltage and experiences the same ripple voltage. The rejection of the PFC output voltage low frequency ripple allows using a smaller bulk capacitance.

Figure 10. Window comparator for rectifying effect detection (Cblock to GND)



Lamp to ground (*Figure 11*): the resistive divider senses the voltage across the lamp. As the L6585DE doesn't have a negative rail, it is necessary to shift the external signal; this can be done (for example) using two Zener diodes connected back-to-back between the EOL pin and the centre of the resistive divider.

The Zener voltages should differ by an amount as close as possible to the double of the internal reference to have a symmetrical detection, in fact:

Let be V_{UP} and V_{DOWN} the maximum allowed values of the DC component of the Lamp Voltage divided by the divider factor K_D, W the window amplitude, V_Z the Zener voltage of a Zener and V_F the forward voltage of the Zener (@ 5.5 μA)

- $V_{UP} = V_{LAMP,MAX}/K_D = V_{REF} + W/2 + V_{Z1} + V_F$
- $V_{DOWN} = V_{LAMP,MIN}/K_D = V_{REF} – W/2 – V_{Z2} – V_F$

It must be:

- $V_{UP} = - V_{DOWN}$

therefore:

- $2\ V_{REF} = V_{Z2} – V_{Z1}$

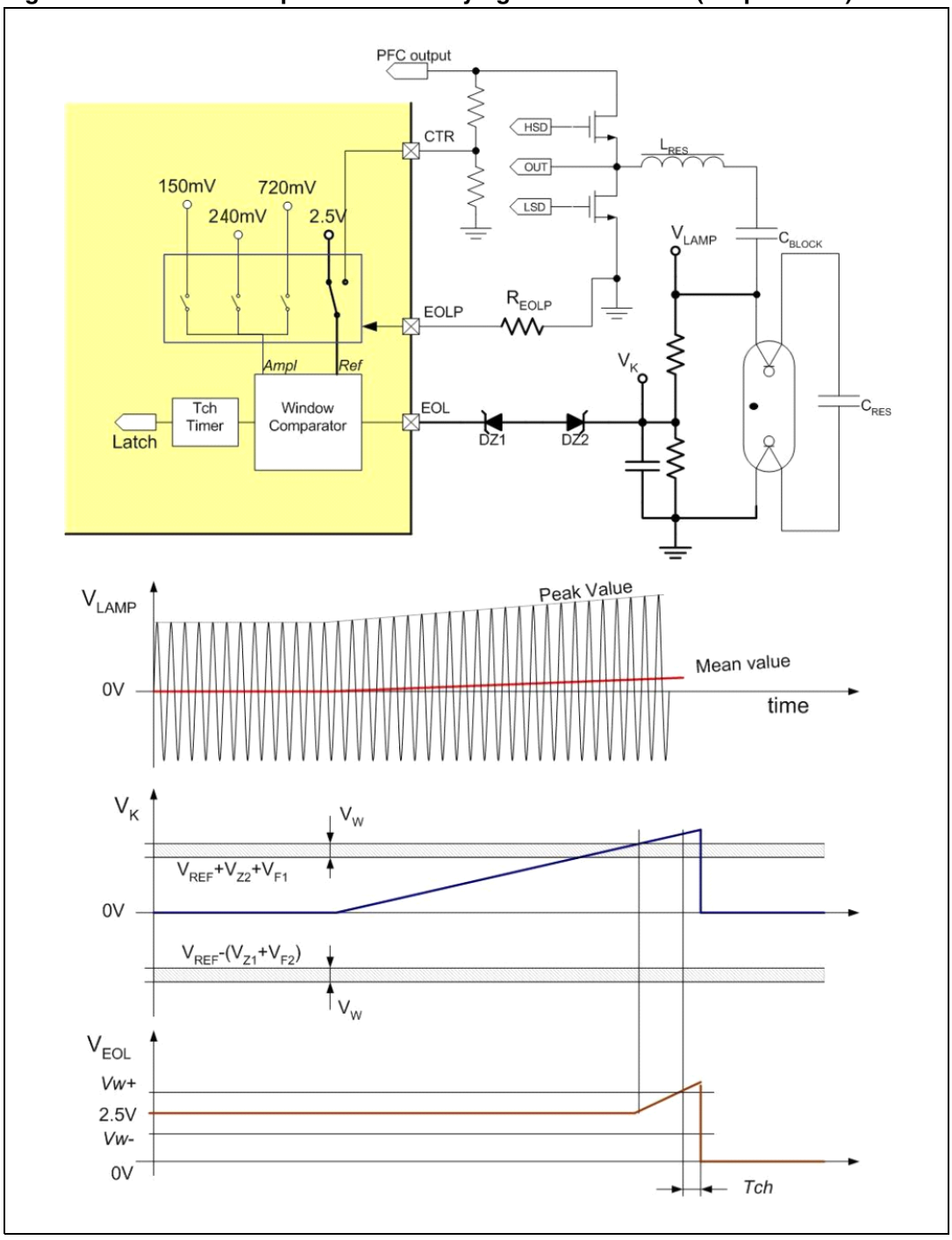
The biasing current available at pin EOL is equal to 5.5 μA then the V_{Z1} Voltage should be greater than 8 V in order to have a more precise EOL threshold.

In this case the window comparator can be referenced to the 2.5 V internal reference as external disturbances don't influence the lamp voltage mean value (Fixed reference configurations).

In the *Figure 11* is shown the case of asymmetric rectification with positive shifting.

To avoid an immediate intervention of the EOL protection, a filtering is introduced: as soon as the voltage at pin EOL goes outside the window of the comparator a Tch cycle is started. The IC is stopped if, at the end of the Tch cycle, the EOL voltage is again outside the limits.

Figure 11. Window comparator for rectifying effect detection (lamp to GND)

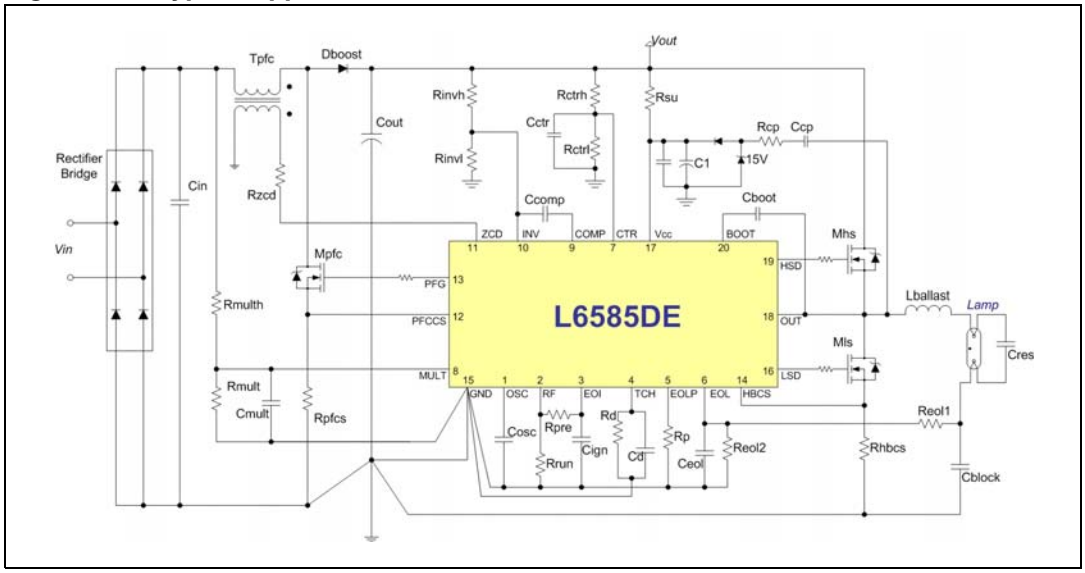


3.3.4 Shutdown

A second comparator, with a threshold equal to 0.8 V, has been introduced on the pin CTR in order to stop the IC if the CTR pin is pulled to ground. If IC is not in latched condition when CTR is pulled down, a new starting sequence is performed as CTR pin voltage is higher than the threshold; this behavior can be used for shutdown.

4 Designing with L6585DE

Figure 12. Typical application



4.1 PFC stage design

Output voltage and dynamic OVP

Output voltage is set designing a voltage divider connected to INV pin:

Equation 2

$$V_{OUT} = 2.52V \cdot \left(1 + \frac{R_{INV,Hi}}{R_{INV,Lo}}\right)$$

The maximum output voltage is set designing a voltage divider connected to CTR pin:

Equation 3

$$V_{OUT,MAX} = 3.4V \cdot \left(1 + \frac{R_{CTR,Hi}}{R_{CTR,Lo}}\right)$$

Both $R_{INV,Hi}$ and $R_{CTR,Lo}$ should be composed by a suitable number of resistors placed in series in order to increase the reliability of the application against over-voltages.

Boost choke design

PFC stage operates in transition mode; for a certain value of input voltage the on time (Ton) is constant over the entire half period of the input voltage.

The frequency changes along the period of the input voltage: in particular the frequency is the lowest when the input voltage reaches its maximum.

Moreover the frequency is higher if the output power is low and the frequency variation changes if input voltage changes.

The internal starter requires a minimum PFC frequency equal to around15 kHz.

Equation 4

$$f_{PFC} = \frac{V_{in}^2}{2 \cdot P_{in} \cdot L} \cdot \left(1 - \frac{\sqrt{2} \cdot V_{in} \cdot \sin(2\pi \cdot f_{mains} \cdot t)}{V_{out}} \right)$$

$$f_{PFC,min} = \frac{V_{in}^2}{2 \cdot P_{in} \cdot L} \cdot \left(1 - \frac{\sqrt{2} \cdot V_{in}}{V_{out}} \right) \geq 15kHz$$

Using Eq.4 with both minimum and maximum value of Vin, the value of L can be selected as the minimum obtained value. Even the maximum frequency should be checked to avoid to absorb too much current from Vcc and to degrade the input performances due to excessive frequency (> 450 kHz) in correspondence to zero input voltage.

The calculation of the maximum frequency is only a rough evaluation of the real frequency; in fact the presence of the THD optimizer reduces the frequency near the crossover of the input voltage.

The maximum current flowing into the choke can be evaluated as twice the maximum input current:

Equation 5

$$I_{L,max} = 2 \cdot \sqrt{2} \cdot \frac{P_{in}}{V_{in,min}}$$

The ohmic power losses will be evaluated considering the RMS value of the current:

Equation 6

$$I_{L,RMS} = \frac{2}{\sqrt{3}} \frac{P_{in}}{V_{in,min}}$$

The choke is realized around of a gapped ferrite core; the core shape has to be selected considering the electrical parameters (Eq.4,5 and 6), the dimensions of the ballast and the availability of the selected core. The core should be made by a material suitable for high frequency operation.

The number of turns and the length of the gap can be calculated as follows (L in uH, Bmax in tesla, Ae in square millimeters and $\mu_0=4\pi*10^{-7}$):

Equation 7

$$\left.\begin{aligned} N &= \frac{I_{max}L}{B_{max}A_e} \\ A_L &= \frac{L}{N^2} \end{aligned}\right\} \rightarrow I_{gap} = 2\times\frac{\mu_0 N^2 A_e}{L}$$

Wire section is selected in order to fit the winding window of the coil former (preferred if slotted).

In order to evaluate the actual copper losses the DC resistance of the winding must be multiplied by a factor that depends on skin effect. Using a wire composed by multiple conductors reduces this factor.

The copper losses can be evaluated as:

Equation 8

$$P_{L,\Omega} = I^2_{L,RMS}\cdot R_{wire,HF}$$

Ferrite losses can be checked on ferrite manufacturer catalogs.

ZCD auxiliary winding must be able to develop the triggering pulse for ZCD pin (V_{arm} = 1.4 V). The voltage across the auxiliary winding will be:

Equation 9

$$V_{aux,zcd} = \left(V_{out} - \sqrt{2}\cdot V_{in}\right) > m\cdot 1.4V$$

The current flowing in ZCD pin must be limited by means of a resistor connected between auxiliary winding and ZCD pin. Although the maximum ZCD pin current is around 5 mA, a smaller value should be chosen in order to limit power dissipation and increase the application reliability.

Equation 10

$$R_{ZCD} = \frac{\sqrt{2}\cdot V_{in,max}}{m\cdot I_{ZCD}}$$

MOSFET selection

PFC MOSFET is to be selected considering the maximum current flowing into the switch, the maximum voltage between drain and source and the maximum allowed losses.

Maximum allowed losses depend on maximum allowed junction temperature; an ambient temperature equal to 70 °C – 80 °C is usually considered.

Power losses can be summarized as follows:

- Conduction losses: due to ohmic resistance of the MOSFET channel during its on state; these losses are prevalent at minimum input voltage.
- Switching losses: experienced only during turn off transitions.
- Capacitive losses: experienced only during turn on transitions when the MOSFET has to discharge the parasitic capacitance present at its drain. These losses are very high at higher input voltages.

Conduction losses are related to $R_{DS(on)}$ and RMS value of the drain current:

Equation 11

$$I^2_{MOS,RMS} = 8\left(\frac{P_{in}}{V_{in,rms}}\right)^2\left[\frac{1}{6} - \frac{4\sqrt{2}}{9\pi}\frac{V_{in,rms}}{V_{OUT}}\right]$$

Considering a maximum conduction losses less than $P_{COND,max}$, the maximum $R_{DS(on)}$, measured at 100 °C, can be found as follows:

Equation 12

$$R_{DS,ON}(max) < \frac{P_{COND,max}}{I^2_{MOS,RMS}}$$

Switching losses are directly related to frequency, to output voltage, to input current and fall time of drain of the MOSFET. The frequency should be averaged over the half period of the mains and the fall time of the MOSFET can be found on MOSFET datasheet.

Equation 13

$$\langle f_{SW} \rangle = \frac{V^2_{in,RMS}}{2 \cdot P_{in} \cdot L}\left(1 - \frac{2\sqrt{2}}{\pi} \cdot \frac{V_{IN,RMS}}{V_{OUT}}\right)$$

Equation 14

$$P_{cross} = t_f \langle f_{sw} \rangle V_{OUT} I_{in,rms} = t_f \langle f_{sw} \rangle V_{OUT} \frac{P_{in}}{V_{in,rms}}$$

Capacitive losses are present only if instantaneous input voltage is greater than half the output voltage. In fact when the inductor current becomes zero the parasitic capacitances seen at the drain node starts to resonate with parasitic inductances causing a damped oscillation whose peak to peak amplitude is equal to V_{OUT} - V_{in}.

When V_{in}<V_{OUT}/2 the drain voltage at MOSFET turn on is almost zero.

The time when input voltage is greater than $V_{OUT}/2$ can be calculated as follows:

Equation 15

$$t_1 = \frac{\arcsin\left(\frac{V_{OUT}}{2 \cdot \sqrt{2} \cdot V_{in,rms}}\right)}{2\pi f_{mains}}$$

$$t_2 = \frac{1}{2f_{mains}} - t_1$$

Within t_2-t_1 interval capacitive losses can be written as:

Equation 16

$$P_{cap} = \langle f_{sw} \rangle \left(3.3 C_{oss} \langle V_{Drain} \rangle^{\frac{3}{2}} + \frac{1}{2}(C_{rss} + C_{oss} + C_{ext}) \langle V_{Drain} \rangle^2 \right)$$

Where

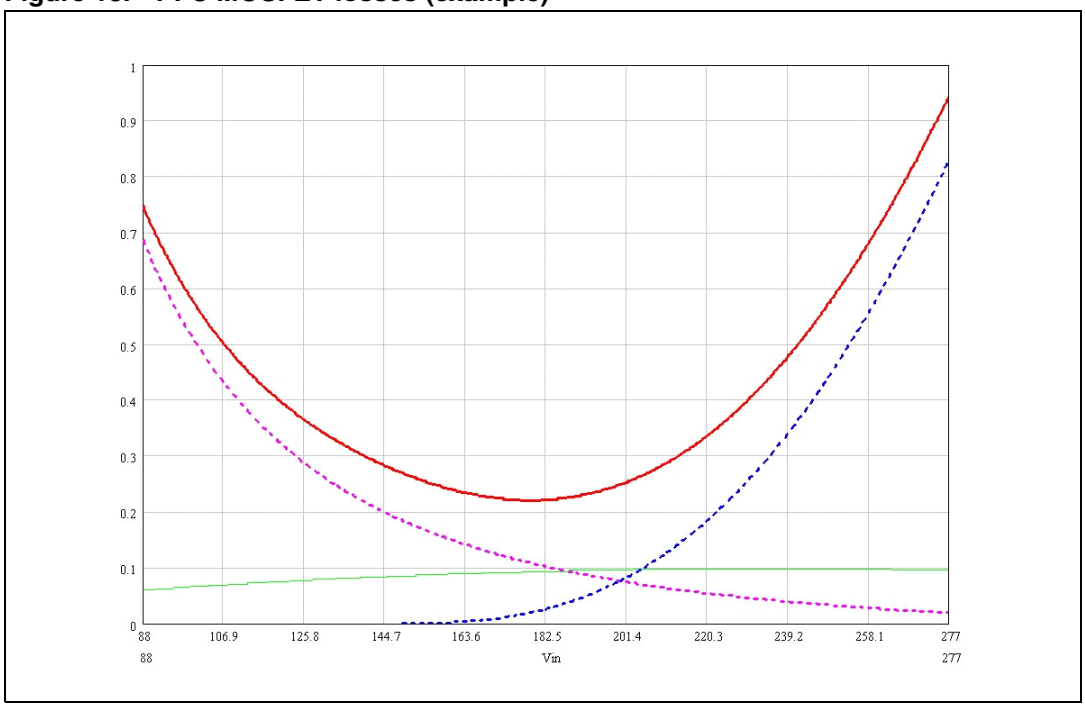
Equation 17

$$V_{Drain,rms} = \sqrt{2f_{mains} \int_{t_1}^{t_2} \left[2\sqrt{2} \cdot V_{in,rms} \sin(\omega t) - V_{out} \right]^2 dt}$$

These losses are greater at higher input voltage.

Figure 13 illustrates an example of calculation in wide range application (Pin = 64 W, MOSFET STx7NM50).

Figure 13. PFC MOSFET losses (example)



Boost diode selection

Boost diode experiences a maximum current equal to maximum boost inductor current, an average current equal to P_{OUT}/V_{OUT} and a RMS current equal to:

Equation 18

$$I_{d,rms} = \sqrt{I_{L,rms}^2 - I_{MOS,RMS}^2} = \frac{4}{3}\frac{\sqrt{2\sqrt{2}}}{\pi}\frac{P_{in}}{\sqrt{V_{OUT}V_{in,rms}}}$$

The maximum reverse voltage must be greater or equal to V_{OUT} and a fast Schottky diode is suggested.

Diode power losses can be calculated using the formula reported in diode datasheet:

Equation 19

$$K_1 \cdot I_{d,AV} + K_2 \cdot I_{d,rms}^2$$

Bulk capacitor selection

Output voltage ripple is due to capacitance value and equivalent series resistor (ESR) of bulk capacitor. ESR value is a function of frequency: higher the frequency, lower the ESR value. The worst ESR will be measured in correspondence of the peak of the input voltage, when the PFC frequency reaches the minimum frequency.

Equation 20

$$\Delta V_{OUT} = \frac{P_{OUT}}{4\pi \cdot f_{mains} \cdot V_{OUT} \cdot C_{out}} + ESR_{@f_{PFC,min}} \cdot I_{C_{out},RMS}$$

Rms value of the bulk capacitor current is:

Equation 21

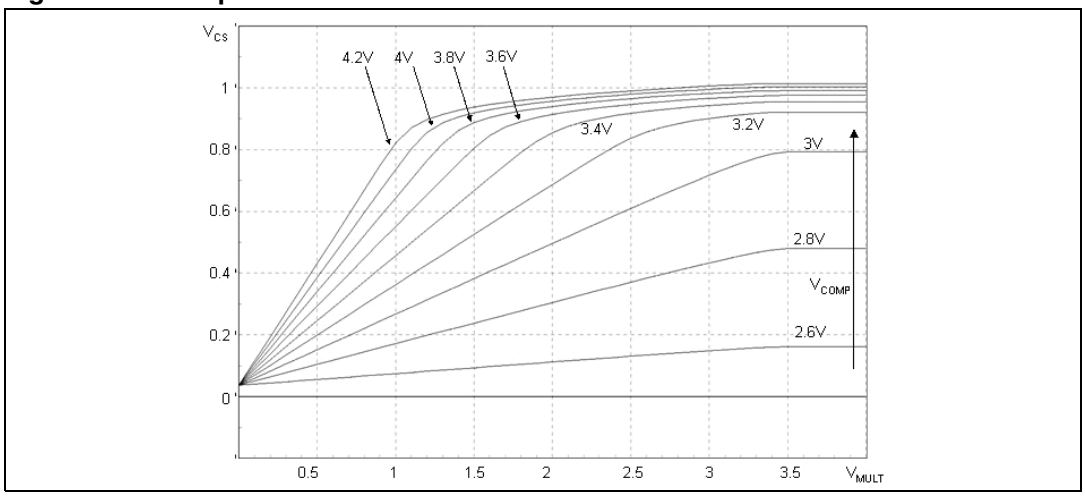
$$I_{C_{OUT},RMS} = \sqrt{\frac{32 \cdot \sqrt{2}}{9\pi} \cdot \frac{P_{in}^2}{V_{in,rms} \cdot V_{OUT}} - \left(\frac{P_{OUT}}{V_{OUT}}\right)^2}$$

Multiplier biasing and PFC current sense resistor selection

The multiplier biasing proceeds as follows (*Figure 14*):

1. Calculate the range of the peak of the input voltage.
2. Consider the characteristic curve that exploits the maximum slope and the point that guarantees, on this curve, a linear behavior. Indicate this point as ($V_{mult,1}$,$V_{CS,1}$)

Figure 14. Multiplier characteristics



3. At minimum input voltage, Vmult had to be biased to $V_{mult,1}$ by means of a voltage divider connected between the rectified input mains and ground. The divider factor is:

Equation 22

$$kp = \frac{V_{mult,1}}{V_{in,min}\big|_{pk}} = \frac{R_{mult,lo}}{R_{mult,lo} + R_{mult,hi}}$$

4. PFC sense resistor is chosen in order to obtain $V_{CS,1}$ at maximum input current (i.e. at minimum input voltage):

Equation 23

$$R_{PFCCS} = \frac{V_{CS,1}}{I_{L,max}} = \frac{V_{CS,1} \cdot V_{in,min}}{2 \cdot \sqrt{2} \cdot P_{in}}$$

5. Check Vmult when Vin assumes its maximum value: this new bias point should lie on the linear segment of a characteristic curve.

The upper resistor value should be obtained using a suitable number of resistors in series in order to increase the reliability of the application. Furthermore a capacitor placed in parallel with lower resistor helps filtering the high frequency components of the signal; the cut frequency of this filter can be placed at ten times the mains frequency, i.e. at 500 Hz.

Error amplifier compensation

Error amplifier compensation design proceeds as follows:

Direct gain of the PFC control loop can be written as (cfr AN966):

Equation 24

$$G(s) = \frac{1}{4} \frac{k_M k_p V_{in,rms}^{\ 2}}{V_{out}} \frac{R_{out}}{R_{PFCCS}} \frac{1}{1 + s\frac{R_{out}C_{out}}{2}}$$

Where R_{out} is the effective resistance of the load (i.e. V_{OUT}^2/P_{OUT}), k_M is the multiplier gain (reported in datasheet) and C_{out} is the bulk capacitor.

In order to compensate the loop and reject the ripple superimposed to the output voltage, the loop gain at 100 Hz should be less than -60 dB. The transfer function of the error amplifier, compensated with a simple capacitor can be written as:

Equation 25

$$G_{comp}(s) = \frac{1}{sC_{comp}R_{invh}}$$

and:

Equation 26

$$G_{loop}(s)\Big| = G(s)\cdot G_{comp}(s)\Big| = \left(\frac{1}{sC_{comp}R_{invh}}\right)\cdot\left(\frac{1}{4}\frac{k_M k_p V_{in,rms}^{\ 2}}{V_{out}}\frac{R_{out}}{R_{pfccs}}\frac{1}{1+s\frac{R_{out}C_{out}}{2}}\right)\Bigg|_{s=2\pi 100Hz} = 0.001$$

Using a high value for R_{invh} the value of C_{comp} is reduced.

Input rectifier

This component is needed to supply the PFC stage with a rectified voltage.

The reverse voltage should be greater than twice $V_{in,max}$, the forward current greater than maximum input current and the power dissipation greater than:

Equation 27

$$P_B = \frac{4}{\sqrt{2}}I_{in,rms(max)}V_F = 2\sqrt{2}\frac{P_{in}}{V_{in,rms(min)}}V_F$$

Input capacitor

At this stage of design the current absorption is impulsive. The mean value of this current is in phase with the input voltage, but the high frequency components have amplitude equal to twice the amplitude of the mean value, therefore can create interferences with nearby electronic equipment. An input filter capacitor must be placed between the rectifier and the PFC stage in order to reduce the high frequency current ripple superimposed to the input current.

Let be *r* the maximum allowed ratio between ripple amplitude and mean value of the input current:

Equation 28

$$C_{in,min} = \frac{I_{in,RMS}}{2\pi\cdot r\cdot\langle f_{sw}\rangle_{min}\cdot V_{in,RMS(min)}} = \frac{P_{in}}{2\pi\cdot r\cdot\langle f_{sw}\rangle_{min}\cdot V_{in,RMS(min)}^{\ 2}}$$

The mean value of the PFC frequency is calculated accordingly with Eq.13.

This capacitor may worsen the overall performance of the PFC stage: in fact the energy stored in it may not be transferred to inductor when the input voltage is near zero. This is the main reason of the introduction of the THD optimizer.

Other input circuitry

The EMI behavior of the circuit needs to be improved with a suitable EMI filter, a fuse with inrush limiter can be introduced for improved reliability against burst and surge events and finally also a surge suppressor (varistor) can be needed.

4.2 Ballast stage design

Resonant network and operating point design

The values of resonant inductor and resonant capacitor and the operating frequencies are chosen in order to:

a) Supply the lamp with correct voltage and current during run mode
b) Maintain lamp voltage lower than Vpre during preheating mode
c) Develop a suitable high voltage across the lamp during the ignition

The resonant network when the lamp is off has a very high Q factor and the resonant frequency is very close to the ideal resonant frequency of an LC resonator.

The relationship between lamp voltage and frequency can be easily found using the Fourier transform and considering the fundamental harmonic of the square wave generated by the half bridge.

Input voltage will be:

Equation 29

$$V_{bal,pk} = \frac{2}{\pi} V_{out}$$

Useful parameters are resonant frequency f_0, characteristic impedance Z_0 and Q factor:

Equation 30

$$\begin{cases} f_0 = \dfrac{1}{2\pi\sqrt{L_{res}C_{res}}} \\ Z_0 = \sqrt{\dfrac{L_{res}}{C_{res}}} \\ Q = \dfrac{R_{lamp}}{Z_0} = \dfrac{V_{run}}{I_{run}Z_0} \end{cases}$$

Where V_{run} and I_{run} are respectively the lamp voltage and lamp current.

The suitable frequencies to obtain the desired operating parameters can be calculated as follows:

Equation 31

$$f_{run} = f_0 \sqrt{\frac{\left(2 - \frac{1}{Q^2}\right) + \sqrt{\left(2 - \frac{1}{Q^2}\right)^2 - 4 + \left(\frac{4V_{out}}{\pi \cdot Z_0 \cdot Q \cdot \sqrt{2} I_{run}}\right)^2}}{2}}$$

$$f_{pre} = \frac{f_0}{2}\left[\frac{2V_{out}}{\pi \cdot Z_0 \cdot I_{pre}} + \sqrt{\left(\frac{2V_{out}}{\pi \cdot Z_0 \cdot I_{pre}}\right)^2 + 4}\right] = (OR) = f_0 \sqrt{1 + \frac{2V_{out}}{\pi V_{pre}}}$$

$$f_{ign} = f_0 \sqrt{1 + \frac{2V_{out}}{\pi \cdot \sqrt{2} \cdot V_{ign}}}$$

L and C are chosen in order to fit the following constraints:

- Preheating voltage has to be less than a value reported on lamp datasheet to avoid early ignition.

Equation 32

$$V_{pre} = \frac{V_{bal,pk}}{\sqrt{\left(\frac{f_{pre}}{f_0} - \frac{f_0}{f_{pre}}\right)^2}} \cdot \frac{f_{res}}{f_{pre}} < V_{pre,max}$$

- In case of current controlled preheating, the Preheating current should be between two values in order to obtain an effective preheating. These two values depend on the preheating time, or, better, on the total energy delivered to the lamp during preheating.

Equation 33

$$I_{pre} = \frac{V_{bal,pk}}{Z_0 \sqrt{\left(\frac{f_{pre}}{f_0} - \frac{f_0}{f_{pre}}\right)^2}} \in \left[I_{ph,min} .. I_{ph,max}\right]$$

- Run frequency should be less than minimum ignition frequency. This frequency is the frequency at which the voltage across the lamp reaches its maximum value (reported on lamp datasheet).

Equation 34

$$V_{ign} = \frac{V_{bal,pk}}{\sqrt{\left(\frac{f_{ign,min}}{f_0} - \frac{f_0}{f_{ign,min}}\right)^2}} \cdot \frac{f_{res}}{f_{ign,min}}$$

Equation 35

$$I_{run} = \frac{V_{bal,pk}}{Z_0\sqrt{Q^2\left(1-\left(\frac{f_{run}}{f_0}\right)^2\right)^2+\left(\frac{f_{run}}{f_0}\right)^2}}$$

An example of characteristic curves is reported in *Figure 15*-A and B

Figure 15. (A) voltage frequency response

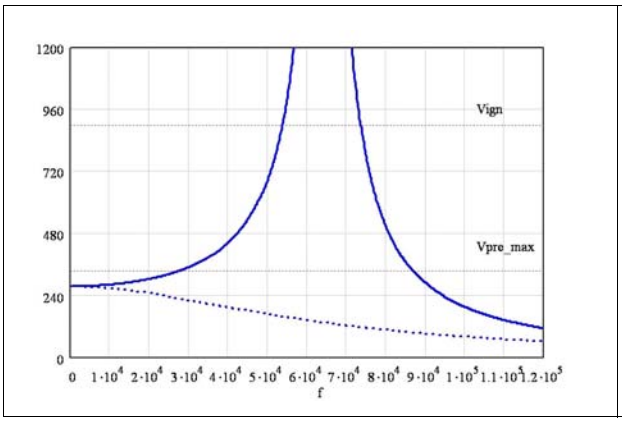
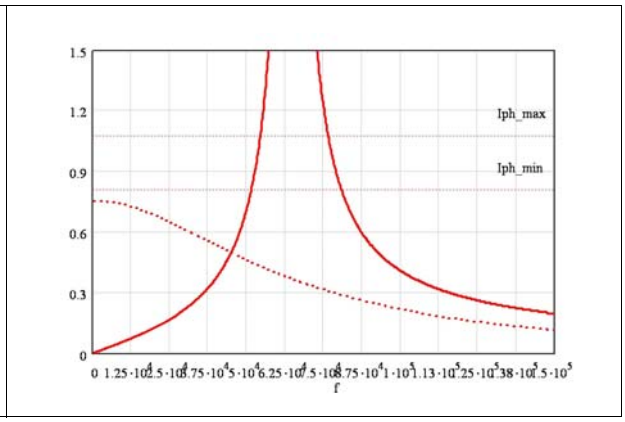


Figure 15. (B) current frequency response



Ballast inductor experiences the maximum current during ignition, when the operating point is very close to the resonance frequency.

Equation 36

$$I_{ballast,ign} = \left(\frac{V_{bal,pk}}{Z_0}\sqrt{\frac{1+\left(Q\frac{f_{ign}}{f_0}\right)}{Q^2\left[1-\left(\frac{f_{ign}}{f_0}\right)^2\right]^2+\left(\frac{f_{ign}}{f_0}\right)^2}}\right)$$

R_{hbcs} must be chosen in order to obtain the minimum ignition voltage across the lamp:

Equation 37

$$R_{HBCS} = \frac{V_{hbcsh}}{I_{ballast,ign}}$$

R_{hbcs} power rating can be calculated considering the RMS value of the low side current during ignition.

In this case the bias point lies at a frequency close to the resonance frequency, therefore the current flowing in resonant network is almost sinusoidal.

This allows the designer to approximate the RMS current to:

Equation 38

$$I_{hbcs,RMS} \approx \frac{I_{lamp,pk}}{2}$$

And the power rating to:

Equation 39

$$P_{hbcs} \approx R_{hbcs} \cdot I^2_{hbcs,RMS}$$

The real maximum inductor current and lamp voltage can be calculated considering the maximum threshold value and the tolerances related with value of Rhbcs and Lres.

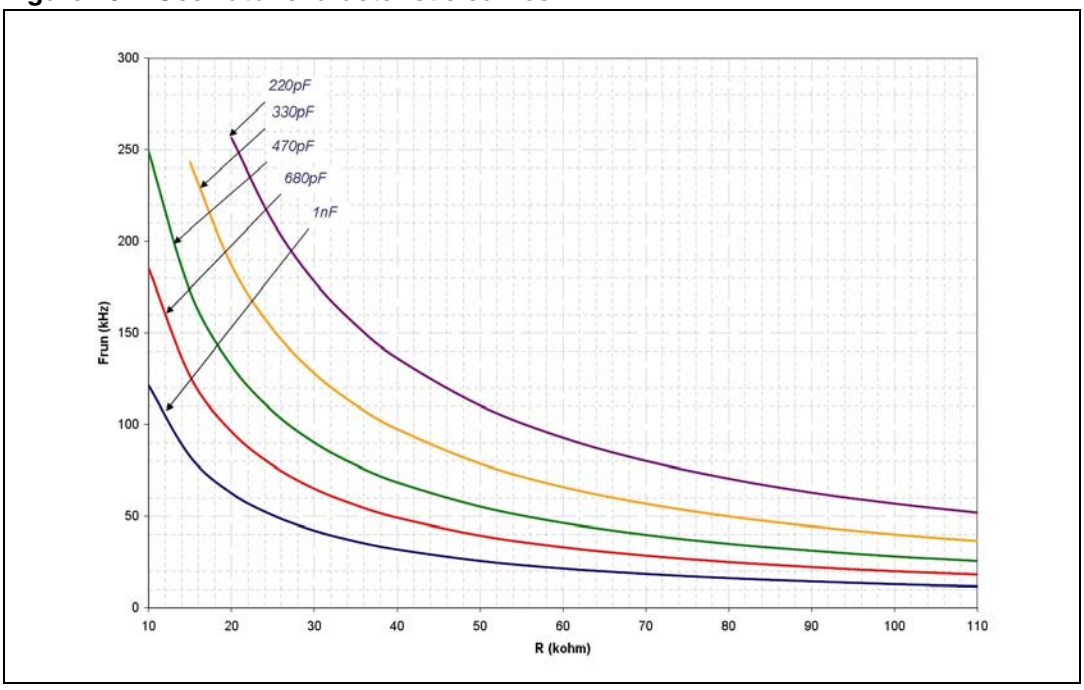
The design of the inductor proceeds as indicated in Eq 7.

The resonance capacitor is preferably a metallized polyester film capacitor. Blocking capacitor is around ten times the resonant one: a value greater or equal to 100 nF for the polyester capacitor is usually chosen.

Parameters setting

In order to fix the run frequency and the preheating frequency, the following curves can be used. Each curve is related with a particular capacitor value, therefore a capacitor value must be firstly chosen. The resistances corresponding Frun and Fpre can be graphically found and are respectively Rrun and the parallel between Rrun and Rpre.

Figure 16. Oscillator characteristic curves



A more accurate procedure can be followed considering that the reported curves can be represented by the following equation (f in kHz and R in kΩ):

Equation 40

$$f = \frac{k}{(R)^e}$$

In particular the constant, *k*, and the exponent, *e*, can be calculated for a given Cosc (expressed in pF) as follows:

Equation 41

$$k = \frac{499.6 \cdot 10^3}{(C_{OSC})^{0.872}}$$

Equation 42

$$e = 1 - \frac{1.33}{(C_{OSC})^{0.581}}$$

Figure 17. (A) k parameter versus Cosc (pF)

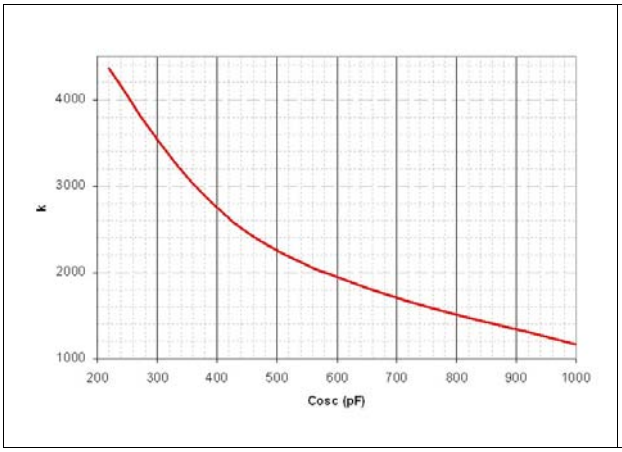
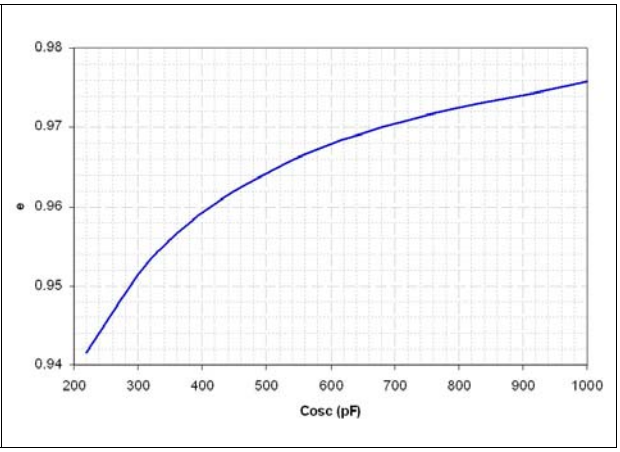


Figure 17. (B) e parameter versus Cosc (pF)



Firstly k and e should be found and then R can be calculated as follows:

Equation 43

$$R_{run} = \left(\frac{k}{f_{run}}\right)^{\frac{1}{e}}$$

$$R_{pre} // R_{run} = \left(\frac{k}{f_{pre}}\right)^{\frac{1}{e}}$$

The ignition time is equal to the time the capacitor Cign is charged by the RF current and the EOI leakage current. A precise calculation of this parameter is not needed. It's approximately equal to:

Equation 44

$$T_{ign} = 3R_{pre}C_{ign}$$

Preheating time and protection time are related to Tch cycle:

Equation 45

$$T_{pre} = 4.63\frac{C_D}{I_{TCH}} + R_D C_D \ln\left(\frac{4.63}{1.5}\right)$$

Equation 46

$$T_{prot} = 269740 \cdot C_D$$

Half bridge design

When resonant network works in inductive region, half bridge MOSFETs switch at zero voltage switching condition.

This implies that high side and low side MOSFETs experience mainly conduction losses because of their on state resistance.

Equation 47

$$P_{cond} = R_{ds,on} \cdot (I_{rms})^2$$

I_{rms} can be considered as per Eq 38 or can be calculated considering that the waveform seen during an on time is a sinusoid having a frequency equal to resonance frequency.

From thermal consideration the maximum $R_{ds,on}$ can be calculated.

In order to drive correctly the high side MOSFET, a suitable boostrap capacitor is needed.

The size of the boostrap capacitor can be calculated considering the allowed V_{gs} drop, the total gate capacitance of the High side MOSFET and the R_{on} of the integrated boostrap diode.

In steady state, during the ON time of the low side transistor the bootstrap capacitor stores charges:

Equation 48

$$Q_{boot} = C_{boot} \cdot V_{cc}$$

During the ON time of the high side transistor, the charges stored in bootstrap capacitor are shared with total gate capacitance, causing a voltage drop:

Equation 49

$$C_{gate} + C_{boot} = \frac{Q_{boot}}{V_{cc} - \Delta V}$$

These charges must be replaced during the subsequent ON time of the low side transistor:

Equation 50

$$T_{boot} = -R_{on}C_{boot} \cdot \left[1 - \ln\left(\frac{\Delta V}{V_{cc}}\right)\right] < \left(\frac{1}{2 \cdot f_{pre}} - T_{DeadTime}\right) = T_{on,min}$$

End of life detection

Blocking capacitor to GND configuration:

In case of blocking capacitor to ground configuration the tracking mode is suggested. In order to set this mode a resistor placed between EOLP and GND is needed: its value has to be chosen as follows:

- 220 kΩ < R_{eolp} < 270 kΩ → V_W = 240 mV
- 22 kΩ < R_{eolp} < 27 kΩ → V_W = 150 mV

EOL pin biasing proceeds as follows:

The blocking capacitor mean voltage is half of the PFC output voltage and the CTR pin voltage is equal to:

Equation 51

$$V_{CTR} = 3.4 \cdot \frac{V_{out}}{V_{OVP}}$$

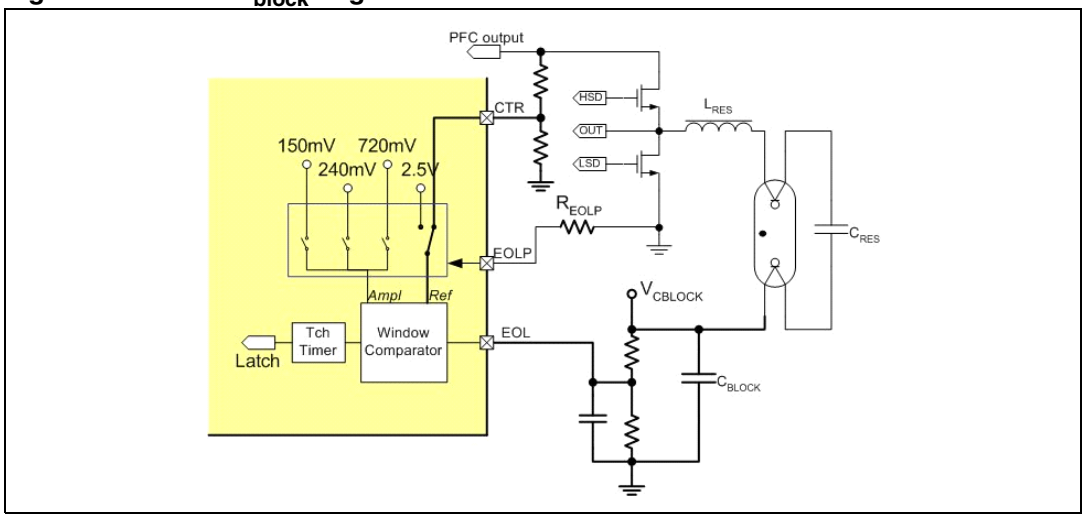
Therefore the voltage divider connected between C_{block} and EOL pin should have a divider factor equal to:

Equation 52

$$k_{eol} = \frac{2 \cdot V_{CTR}}{V_{out}} = \frac{6.8}{V_{OVP}}$$

A capacitor placed in parallel with the lower resistor and placed near the IC helps to keep low the high frequency residual noise.

Figure 18. EOL - C_{block} to ground



Lamp to GND configuration:

In case of lamp to ground configuration the fix reference mode is suggested.

In order to set this mode a resistor placed between EOLP and GND is needed: its value has to be chosen as follows:

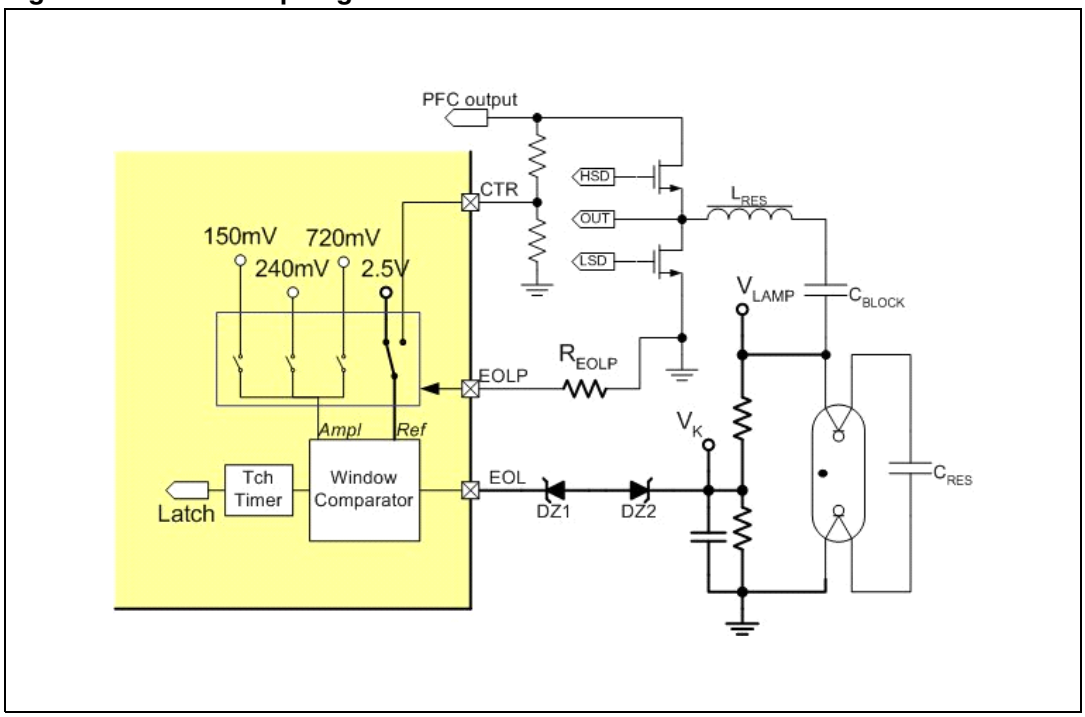
- 75 kΩ < R_{eolp} < 91kΩ → window amplitude = 240 mV
- 620 kΩ < R_{eolp} → window amplitude = 720 mV

The EOL pin biasing proceeds as follows:

A voltage shift is needed in order to detect a null value with a positive referenced comparator: two Zener diodes are requested.

The current capability of EOL pin is equal to 5.5 µA, therefore the minimum Zener voltage that guarantees accuracy of the measurement is 8 V.

Figure 19. EOL - lamp to ground



Consider the case of positive going lamp voltage mean value (V_K): the maximum V_K allowed value is equal to:

Equation 53

$$V_K|_{max} = 2.5 + V_W + V_{z1} + V_{F2}$$

In the opposite case it will be:

Equation 54

$$V_K|_{min} = 2.5 - V_W - V_{z2} - V_{F1}$$

In order to have a symmetrical behavior, the absolute values of the two voltages have to be equal.

This brings to the following relation:

Equation 55

$$V_K|_{max} = \left(-V_K|_{min}\right)$$
$$\Rightarrow 2.5 + V_W + V_{z1} + V_{F2} = -2.5 + V_W + V_{z2} + V_{F1}$$
$$\Rightarrow 2 \cdot 2.5V = V_{z2} - V_{z1}$$

The difference of the Zener voltages has to be equal to 5V: twice the reference voltage.

The maximum deviation of the mean voltage of the lamp, $V_{lamp,EOL}$, depends on the lamp type (e.g. is 15 V for T5-54W lamp).

The following relation can be used to calculate the correct value of the divider's resistors (R_{Ehi} and R_{Elo})

Equation 56

$$V_K\big|_{max} = V_{lamp,EOL} - R_{Ehi} \cdot (I_{RElo} + I_{EOL})$$

$$V_K\big|_{max} = V_{lamp,EOL} - \frac{V_{lamp,EOL} \cdot R_{Ehi}}{R_{Ehi} + R_{Elo}} - R_{Ehi} \cdot 5.5\mu A$$

The value of filtering capacitor should be calculated in order to have a cutoff frequency equal to at least one hundreds of run frequency.

IC power supply design

L6585DE can be supplied by means of either external source, auxiliary winding on PFC choke or charge pump connected to the middle point of half bridge. The most used method is the charge pump connected to the middle point of the half bridge.

The charge pump must be able to deliver the correct current to the IC. I_{CC} depends on both half bridge and PFC driver switching activities. Typical values of I_{CC} are reported on *Figure 20*.

The current is delivered by the capacitor during the edges of the middle point of the half bridge. The slope of these edges is also related to the recovery time of the body diode of the MOSFETs and to the capacitor itself. Assuming a linear slope the instantaneous current delivered by the capacitor will be:

Equation 57

$$I_{cp,pk} = C_{cp} \frac{V_{OUT}}{T_{rise}}$$

Equation 58

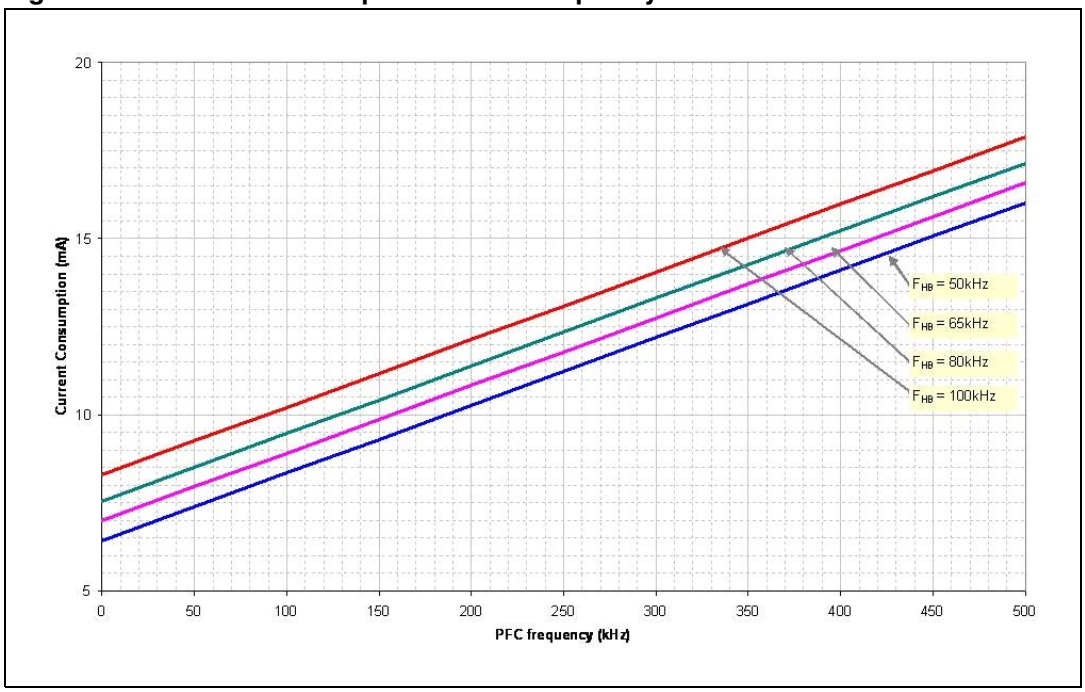
$$I_{cp} = I_{cp,pk} \cdot T_{rise} \cdot f_{run} \geq I_{cc}$$

The diode connected to ground is a Zener diode (15 V is the suggested value): it limits the voltage across the Vcc pin avoiding an extra stress of the internal active clamp. In order to limit the current flowing into this diode, when it is directly biased, a low value resistor is placed in series with the capacitor.

A bigger capacitor (>1 µF) and a 100 nF ceramic capacitor placed near the IC are needed to filter the Vcc voltage.

At start up the current is sunk from rectified mains and delivered to the IC through a resistor path. This resistor is chosen in order to guarantee the minimum quiescent current required by L6585DE (370 µA). Its value influences also the start-up time because it had to charge the electrolytic capacitor connected to Vcc.

Figure 20. Current consumption vs PFC frequency



4.3 PCB hints

The following rules, considered during the PCB design, help to optimize the performance of the L6585DE.

1. In a board containing both PFC and Ballast section four different ground potentials are present:
   a) PFC signal ground,
   b) PFC power ground
   c) Ballast signal ground and
   d) Ballast power ground.

These traces are usually kept separate and connected together in correspondence of a low impedance node (the negative terminal of bulk capacitor). A similar rule has to be followed in the L6585DE: power grounds are to be kept separate and connected to the negative terminal of the bulk capacitor, signal grounds should be firstly routed to the pin GND (15) and then the pin 15 is connected to the negative terminal of bulk capacitor. It is very important that the ground trace relevant to C_{OSC}, R_{RF} and C_{PRE} is connected directly to the GND pin as shortly as possible.

2. Ballast PCBs are usually long and narrow, therefore current loops are to be minimized in order to reduce the electromagnetically induced interference between PFC stage and Ballast Stage. This is very important when wide range application has to be implemented.
3. Regions surrounding the gap of the chokes are usually very noisy therefore signal and ground traces shouldn't pass underneath these regions.
4. Traces that connect the gates of the MOSFETs, the OUT pin and the charge pump components are affected by voltages that vary with very fast edges. They can capacitively induce noise to closest traces. Therefore if a signal has to pass near these nodes an increased distance between traces or, eventually, a ground shield has to be considered.
5. Ground pin of shunt components should be placed as close as possible to star connection point or, at least, close together, this avoids errors reading the voltage across them and current sense traces has to be kept as short as possible in order to avoid HF noise induction. In the second case is preferable to connect signal GND to the ground of the shunts instead of the star point.
6. Bootstrap capacitor and Vcc ceramic capacitor have to be placed as close as possible to relevant pins.
7. Error amplifier feedback network must be small and placed near the IC in order to reduce any loop that can couple radio interference.
8. The drain of the PFC MOSFET, the anode of Boost Diode and the PFC choke are connected together as close as possible. In fact this node experienced very fast edges and also very high currents.

5 Revision history

Table 2. Document revision history

Date	Revision	Changes
26-Mar-2009	1	Initial release

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